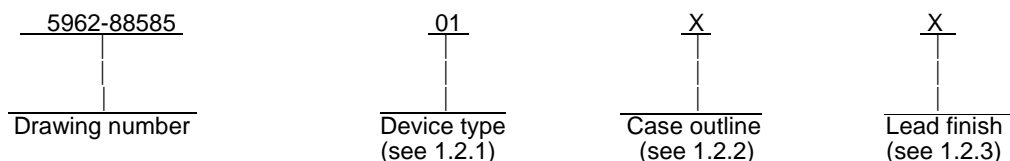


REVISIONS																				
LTR	DESCRIPTION										DATE (YR-MO-DA)				APPROVED					
A	Added device type 02. Added footnote 9 to table I for IIL3, IIL4, IIH3, and IIH4. Figure 1; Made corrections to case outlines X and Y. Redrew entire document. -sld										01-12-10				Raymond Monnin					
B	Figure 1, case outline X; corrected the dimension L in the conversion table from .024 (0.61 mm) min and .026 (0.66 mm) max to .240 (6.10 mm) min and .260 (6.60 mm) max. -sld										02-02-25				Raymond Monnin					
THE ORIGINAL FIRST SHEET OF THIS DOCUMENT HAS BEEN REPLACED																				
REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B										
SHEET	15	16	17	18	19	20	21	22	23	24										
REV STATUS				REV		B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14	
PMIC N/A				PREPARED BY Robert M. Heber							DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dscc.dla.mil									
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Ray Monnin																
				APPROVED BY Michael A. Frye							MICROCIRCUIT, HYBRID, LINEAR, MIL-STD-1553 BUS CONTROLLER, RTU, AND MONITOR UNIT									
				DRAWING APPROVAL DATE 88-12-20																
				REVISION LEVEL B							SIZE A	CAGE CODE 67268	5962-88585							
											SHEET 1 OF 24									

1. SCOPE

1.1 Scope. This drawing describes device requirements for class H hybrid microcircuits to processed in accordance with MIL-PRF-38534.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	BUS-65600, CT2565	MIL-STD-1553, BUS controller, RTU, and monitor unit
02	CT2565-001	MIL-STD-1553, BUS controller, RTU, and monitor unit

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	78	Dual-in-line
Y	See figure 1	82	Flat pack

1.2.3 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range (V_{IN})	GND -0.3 V dc to V_{CC} +0.3 V dc
Supply current (I_{CC})	70 mA 2/
Power dissipation (P_D)	385 mW 2/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal rise, junction-to-case (ΔT_J)	+5°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Minimum logic high input voltage (V_{IH})	2.4 V dc
Maximum logic low input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to 125°C
Operating frequency (F_{OP})	12.0 MHz

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Applies up to $T_C = +125^\circ\text{C}$ with all outputs open.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1553 - Aircraft Internal Time Division Command/Response Multiplex Data Bus.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38534.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Timing diagram(s). The timing diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified		Group A subgroups 1/	Device types	Limits		Unit
						Min	Max	
Supply current	I _{CC}	V _{CC} = 5.5 V, F _{IN} = 12 MHz, measured at pin 20 for case outline X and pin 40 for case outline Y with all outputs open		1, 2, 3	01,02		70	mA
High level output voltage 2/	V _{OH1}	V _{CC} = 4.5 V, V _{IH} = 2.5 V, V _{IL} = 0.4 V	I _{OH} = -5.2 mA	1,2,3	01,02	2.7		V
High level output voltage 3/	V _{OH2}		I _{OH} = -40 μA	1,2,3	01,02	2.7		
High level output voltage 4/	V _{OH3}		I _{OH} = -80 μA	1,2,3	01,02	2.7		
Low level output voltage 2/	V _{OL1}	V _{CC} = 4.5 V, V _{IH} = 2.5 V, V _{IL} = 0.4 V	I _{OL} = 5.2 mA	1,2,3	01,02		0.4	V
Low level output voltage 3/	V _{OL2}		I _{OL} = 1.6 mA	1,2,3	01,02		0.4	
Low level output voltage 4/	V _{OL3}		I _{OL} = 2.4 mA	1,2,3	01,02		0.4	
High level input current 5/	I _{IH1}	V _{CC} = 5.5 V, V _{IN} = 2.5 V		1,2,3	01,02	-20	+20	μA
High level input current 6/	I _{IH2}			1,2,3	01,02	-10	+10	
High level input current 7/	I _{IH3} 9/			1,2,3	01,02	0.0	-250	
High level input current 8/	I _{IH4} 9/			1,2,3	01,02	0.0	-800	
Low level input current 5/	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.4 V		1,2,3	01,02	-20	+20	μA
Low level input current 6/	I _{IL2}			1,2,3	01,02	-10	+10	
Low level input current 7/	I _{IL3} 9/			1,2,3	01,02	0.0	-500	
Low level input current 8/	I _{IL4} 9/			1,2,3	01,02	0.0	1.6	mA
Functional tests 10/		V _{CC} = 4.5 V, V _{IH} = 2.5 V, V _{IL} = 0.4 V, f _{IN} = 12 MHz		7,8	01,02			Pass/ fail
Maximum clock frequency	f _{MAX}	50% duty cycle 11/		9,10,11	01,02		12.0	MHz
DELAY TIMING								
$\overline{\text{BUSGRNT}}$ delay, CMD word	t _{d1}	V _{CC} = 4.5 V, V _{IH} = 2.5 V, V _{IL} = 0.4 V, f _{IN} = 12 MHz, See figure 3 11/ 12/		9,10,11	01,02		1.5	μs
$\overline{\text{BUSGRNT}}$ delay, TX data word	t _{d2}			9,10,11	01,02		15.5	μs
$\overline{\text{BUSGRNT}}$ delay, RX data	t _{d3}			9,10,11	01,02		2.33	μs
$\overline{\text{BUSGRNT}}$ to $\overline{\text{BUSACK}}$ delay (RTU handshake)	t _{d4}			9,10,11	01,02		250	ns
See footnotes at end of table.								
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000				SIZE A	REVISION LEVEL B		5962-88585	
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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups 1/	Device types	Limits		Unit
					Min	Max	
DELAY TIMING - CONTINUED							
$\overline{\text{BUSACK}}$ to $\overline{\text{OE}}$ delay	t _{d5}	V _{CC} = 4.5 V, V _{IH} = 2.5 V, V _{IL} = 0.4 V, f _{IN} = 12 MHz, See figure 3 11/ 12/	9,10,11	01,02		25	ns
$\overline{\text{OE}}$ to $\overline{\text{CS}}$ delay	t _{d6}		9,10,11	01,02		25	ns
$\overline{\text{CS}}$ to $\overline{\text{ADRINC}}$ delay	t _{d7}		9,10,11	01,02		110	ns
$\overline{\text{BUSACK}}$ to $\overline{\text{WR}}$ delay (BC write)	t _{d8}		9,10,11	01,02	300	378	ns
$\overline{\text{WR}}$ to $\overline{\text{CS}}$ delay	t _{d9}		9,10,11	01,02		25	ns
$\overline{\text{NBGRNT}}$ to LMC, WC, T/R delay	t _{d10}		9,10,11	01,02	500	667	ns
LMC to $\overline{\text{ILLCMD}}$ latch	t _{D11}		9,10,11	01,02	250		ns
$\overline{\text{NBGRNT}}$ to $\overline{\text{INCMD}}$ delay	t _{D12}		9,10,11	01,02	0.9	1.1	μs
$\overline{\text{BUSACK}}$ to $\overline{\text{SOM}}$ delay	t _{D13}		9,10,11	01,02	140	190	ns
$\overline{\text{NBGRNT}}$ low to status latch	t _{D14}		9,10,11	01,02	2.5	3.5	μs
$\overline{\text{CS}}$ to $\overline{\text{ADRINC}}$ delay (RTU read)	t _{D15}		9,10,11	01,02		110	ns
$\overline{\text{BUSACK}}$ to $\overline{\text{WR}}$ delay (RTU write)	t _{D16}		9,10,11	01,02	140	225	ns
$\overline{\text{WR}}$ to $\overline{\text{CS}}$ delay (RTU write)	t _{D17}		9,10,11	01,02		25	ns
$\overline{\text{BUSREQ}}$ to $\overline{\text{BUSGRNT}}$ delay	t _{D18}		9,10,11	01,02		2.0	μs
$\overline{\text{BUSGRNT}}$ to $\overline{\text{BUSACK}}$ delay (MT transfer)	t _{D19}		9,10,11	01,02		250	ns
$\overline{\text{BUSACK}}$ to $\overline{\text{WR}}$ delay (MT transfer)	t _{D20}		9,10,11	01,02	300	378	ns

See footnotes at end of table.

**STANDARD
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DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤+125°C unless otherwise specified	Group A subgroups 1/	Device types	Limits		Unit
					Min	Max	
PULSE WIDTH TIMING							
$\overline{\text{BUSREQ}}$ pulse width (RTU handshake)	t _{PW1}	V _{CC} = 4.5 V, V _{IH} = 2.5 V, V _{IL} = 0.4 V, f _{IN} = 12 MHz, See figure 3 10/ 12/	9,10,11	01,02	667		ns
$\overline{\text{BUSACK}}$ pulse width (RTU handshake)	t _{PW2}		9,10,11	01,02	475	600	ns
$\overline{\text{CS}}$, ($\overline{\text{OE}}$) pulse width (BC read)	t _{PW3}		9,10,11	01,02	640	690	ns
$\overline{\text{ADRINC}}$ pulse width	t _{PW4}		9,10,11	01,02	60	110	ns
$\overline{\text{CS}}$ and $\overline{\text{WR}}$ pulse width (BC write)	t _{PW5}		9,10,11	01,02	140	190	ns
$\overline{\text{NBGRNT}}$ pulse width	t _{PW6}		9,10,11	01,02	140	190	ns
$\overline{\text{SOM}}$ pulse width	t _{PW7}		9,10,11	01,02	140	190	ns
$\overline{\text{CS}}$, $\overline{\text{OE}}$, and $\overline{\text{BUSACK}}$ pulse width (RTU read)	t _{PW8}		9,10,11	01,02	475	600	ns
$\overline{\text{CS}}$ and $\overline{\text{WR}}$ pulse width (RTU write)	t _{PW9}		9,10,11	01,02	140	190	ns
$\overline{\text{BUSREQ}}$ pulse width (BC handshake)	t _{PW10}		9,10,11	01,02	752		ns
$\overline{\text{BUSGRNT}}$ pulse width (BC handshake)	t _{PW11}		9,10,11	01,02	250		ns
$\overline{\text{BUSACK}}$ pulse width (BC handshake)	t _{PW12}		9,10,11	01,02	640	690	ns
$\overline{\text{BUSGRNT}}$ pulse width (MT transfer)	t _{PW13}		9,10,11	01,02	250		ns
See footnotes at end of table.							
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000			SIZE A			5962-88585	
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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤+125°C unless otherwise specified	Group A subgroups 1/	Device types	Limits		Unit
					Min	Max	
SET-UP TIMING							
BC read data set-up time	t _{S1}	V _{CC} = 4.5 V, V _{IH} = 2.5 V, V _{IL} = 0.4 V, f _{IN} = 12 MHz, See figure 3 10/ 12/	9,10,11	01,02		250	ns
BC write data valid set-up time	t _{S2}		9,10,11	01,02	100		ns
CMD valid set-up time	t _{S3}		9,10,11	01,02	100		ns
RTU read data set-up time	t _{S4}		9,10,11	01,02		166	ns
RTU write data valid set-up prior to leading edge of <u>WR</u>	t _{S5}		9,10,11	01,02	100		ns
ID word valid set-up time	t _{S6}		9,10,11	01,02	100		ns

See footnotes on next page.

**STANDARD
MICROCIRCUIT DRAWING**

 DEFENSE SUPPLY CENTER COLUMBUS
 COLUMBUS, OHIO 43216-5000

 SIZE
A

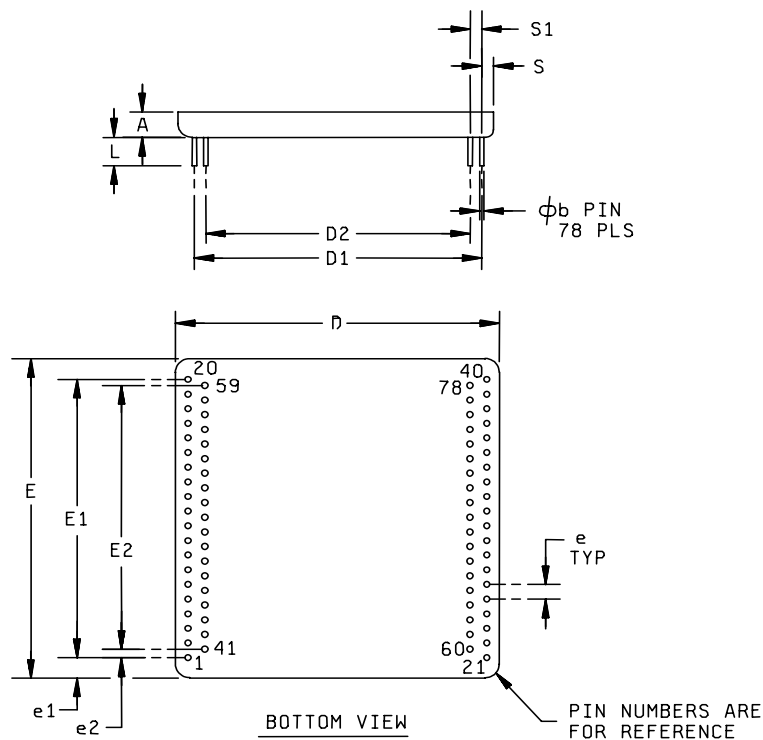
 REVISION LEVEL
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TABLE I. Electrical performance characteristics - Continued.

- 1/ All Group A subgroup testing may be performed concurrently.
- 2/ Measured at the following pins:
Case X: Pins 14, 21 - 28, 54, and 60 - 67.
Case Y: Pins 28, 29, and 66 - 81.
- 3/ Measured at the following pins:
Case X: Pins 3 - 5, 9, 12, 13, 15 -19, 29, 30, 42 - 44, 46, 49, 51 - 53, 55, 57, 59, 68, 71, 75, and 78.
Case Y: Pins 5 - 10, 18, 23 - 27, 30 - 32, 34 - 36, 38, 39, 44, 50, 58, and 63 - 65.
- 4/ Measured at the following pins:
Case X: Pins 31, 37, 69, and 76.
Case Y: Pins 48, 49, 61, and 62.
- 5/ Measured at the following pins:
Case X: Pins 1 and 45.
Case Y: Pins 2 and 11.
- 6/ Measured at the following pins:
Case X: Pins 2, 6 - 8, 10, 21 - 28, 32, 36, 38, 39, 41, 47, 48, 60 - 67, 70, and 77.
Case Y: Pins 3, 4, 12, 14 - 17, 20, 45 - 47, 51, 59, 60, and 66 - 81.
- 7/ Measured at the following pins:
Case X: Pins 33 and 58.
Case Y: Pins 37 and 57.
- 8/ Measured at the following pins:
Case X: Pins 34, 35, and 72 - 74.
Case Y: Pins 52 - 56.
- 9/ For device type 02, case X, pins 33 - 35 and 72 - 74, and case Y pins 52 - 57 have a 0.01 μ F capacitor to ground.
- 10/ Functional tests performed to verify functionality of the device as a MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (BM). These tests shall be a part of the manufacturer's test tapes and shall be made available to the acquiring activity upon request.
- 11/ If not tested, parameter(s) shall be guaranteed to the limits specified in table I.
- 12/ All timing characteristics measured at 2.7 V and 0.4 V, unless otherwise specified.

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Case outline X



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		6.35		.250
Φb	0.33	0.58	.013	.023
D		47.50		1.870
D1	41.78	42.04	1.645	1.655
D2	37.97	38.23	1.495	1.505
E		53.34		2.100
E1	48.13	48.39	1.895	1.905
E2	45.59	45.85	1.795	1.805
e	2.54 TYP		.100 TYP	
e1	2.41	2.67	.095	.105
e2	1.14	1.40	.045	.055
L	6.10	6.60	.240	.260
S	1.78	2.03	.070	.080
S1	1.91 TYP		.075 TYP	

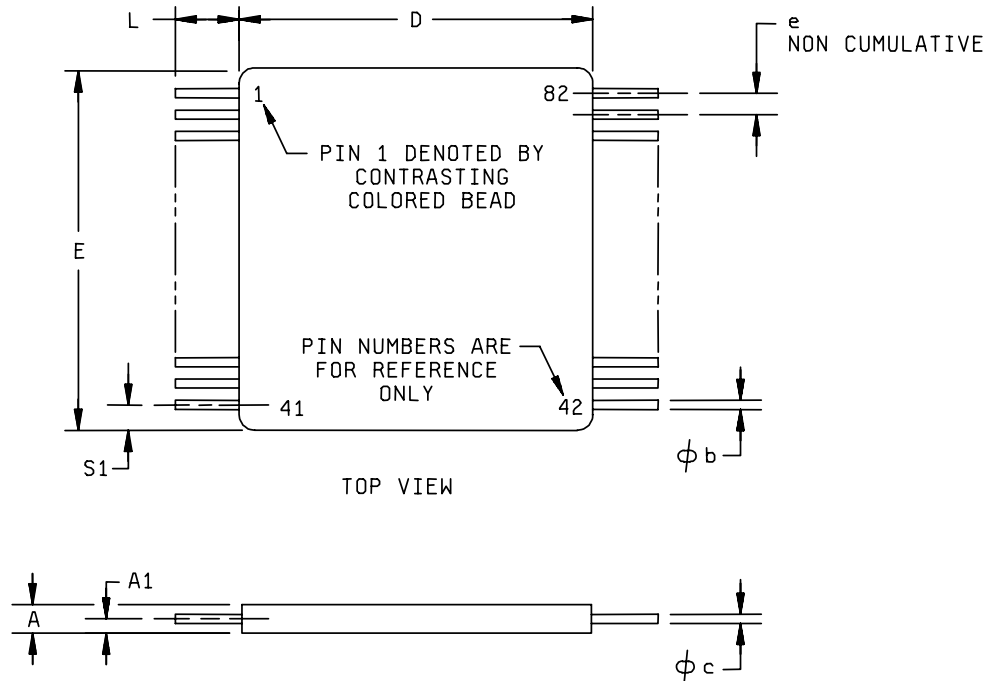
NOTES:

1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s).

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Case outline Y



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.72		.186
A1	2.03 REF		.080 REF	
Φb	0.30	0.46	.012	.018
Φc	0.20	0.30	.008	.012
D	40.51	40.77	1.595	1.605
E	55.50	55.75	2.185	2.195
e	1.27 TYP		.050 TYP	
L	10.16		.400	
S1	2.41 REF		.095 REF	

NOTES:

1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s) - Continued.

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Device types	All		Device types	All	
Case outline	X		Case outline	X	
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	RT/ \overline{BC}	27	DB12	53	WC4
2	\overline{MT}	28	DB14	54	TXINH A
3	\overline{STATEN}	29	LWORD	55	LMC
4	$\overline{TIMEOUT}$	30	\overline{MSGERR}	56	\overline{TESTIN}
5	\overline{HSFAIL}	31	TXDATA A	57	\overline{EOM}
6	$\overline{DBACCEPT}$	32	$\overline{RXDATA A}$	58	\overline{BUFENA}
7	\overline{SSFLAG}	33	RTADP	59	\overline{BUSACK}
8	\overline{SVCREQ}	34	RTAD1	60	DB1
9	\overline{INCMD}	35	RTAD3	61	DB3
10	\overline{SSER}	36	\overline{RESET}	62	DB5
11	$\overline{TESTOUT}$	37	$\overline{TXDATA B}$	63	DB7
12	WC1	38	RXDATA B	64	DB9
13	WC3	39	12MHz	65	DB11
14	TXINH B	40	GND	66	DB13
15	T/ \overline{R}	41	$\overline{BCSTART}$	67	DB15 (MSB)
16	$\overline{CHA / CHB}$	42	\overline{NBGRNT}	68	$\overline{STATERR}$
17	\overline{CS}	43	\overline{BITEN}	69	$\overline{TXDATA A}$
18	\overline{OE}	44	\overline{WR}	70	RXDATA A
19	\overline{BUSREQ}	45	$\overline{BUSGRNT}$	71	$\overline{NO DT}$
20	+5 V	46	$\overline{LOOPERR}$	72	RTAD0
21	DB0 (LSB)	47	\overline{SSBUSY}	73	RTAD2
22	DB2	48	\overline{ILLCMD}	74	RTAD4
23	DB4	49	\overline{ADRINC}	75	$\overline{BCSTRCV}$
24	DB6	50	CHASSIS	76	TXDATA B
25	DB8	51	WC0	77	$\overline{RXDATA B}$
26	DB10	52	WC2	78	\overline{SOM}

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-88585
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Device types	All		Device types	All	
Case outline	Y		Case outline	Y	
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	29	TXINH A	57	RTADP
2	RT/ \overline{BC}	30	T/ \overline{R}	58	$\overline{NO\ DT}$
3	$\overline{BCSTART}$	31	LMC	59	$\overline{RXDATA\ A}$
4	\overline{MT}	32	$\overline{CHA\ /CHB}$	60	RXDATA A
5	\overline{NBGRNT}	33	\overline{TESTIN}	61	TXDATA A
6	\overline{STATEN}	34	\overline{CS}	62	$\overline{TXDATA\ A}$
7	\overline{BITEN}	35	\overline{EOM}	63	\overline{MSGERR}
8	$\overline{TIMEOUT}$	36	\overline{OE}	64	$\overline{STATERR}$
9	\overline{WR}	37	\overline{BUFENA}	65	LWORD
10	\overline{HSFAIL}	38	\overline{BUSREQ}	66	DB15 (MSB)
11	$\overline{BUSGRNT}$	39	\overline{BUSACK}	67	DB14
12	$\overline{DBACCEPT}$	40	+5 V	68	DB13
13	$\overline{LOOPERR}$	41	NC	69	DB12
14	\overline{SSFLAG}	42	NC	70	DB11
15	\overline{SSBUSY}	43	GROUND	71	DB10
16	\overline{SVCREQ}	44	\overline{SOM}	72	DB9
17	\overline{ILLCMD}	45	12MHz	73	DB8
18	\overline{INCMD}	46	$\overline{RXDATA\ B}$	74	DB7
19	\overline{ADRINC}	47	RXDATA B	75	DB6
20	\overline{SSER}	48	TXDATA B	76	DB5
21	CHASSIS	49	$\overline{TXDATA\ B}$	77	DB4
22	$\overline{TESTOUT}$	50	$\overline{BCSTRCV}$	78	DB3
23	WC0	51	\overline{RESET}	79	DB2
24	WC1	52	RTAD4	80	DB1
25	WC2	53	RTAD3	81	DB0 (LSB)
26	WC3	54	RTAD2	82	NC
27	WC4	55	RTAD1		
28	TXINH B	56	RTAD0		

FIGURE 2. Terminal connections - Continued.

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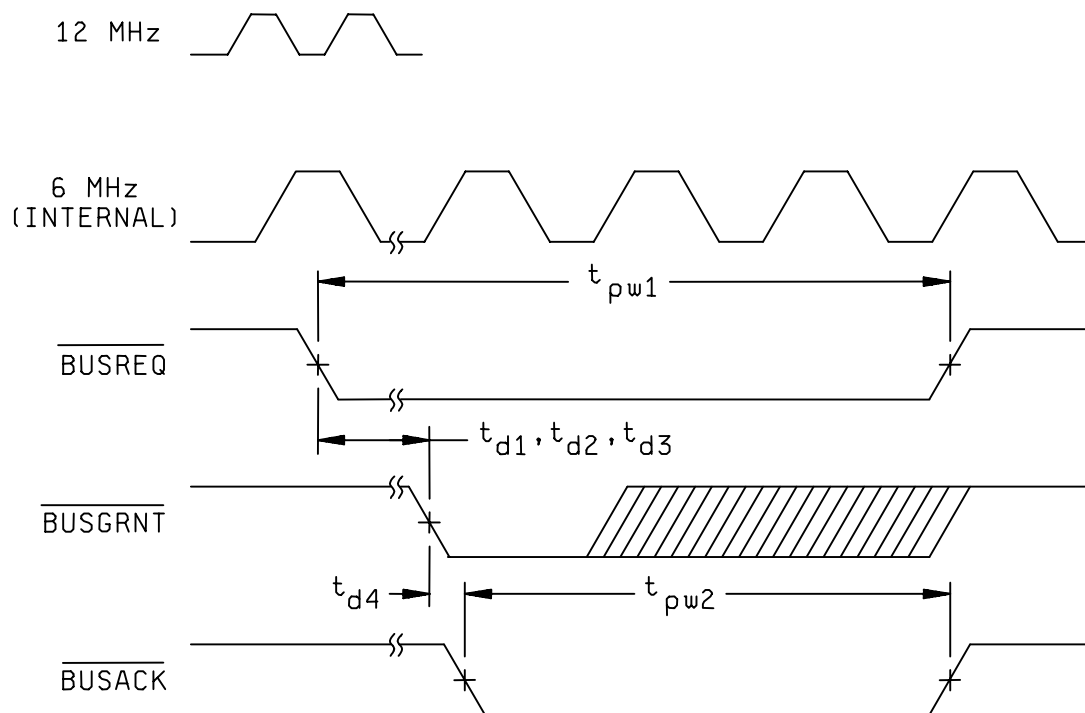


FIGURE 3. Timing diagram - RTU handshake.

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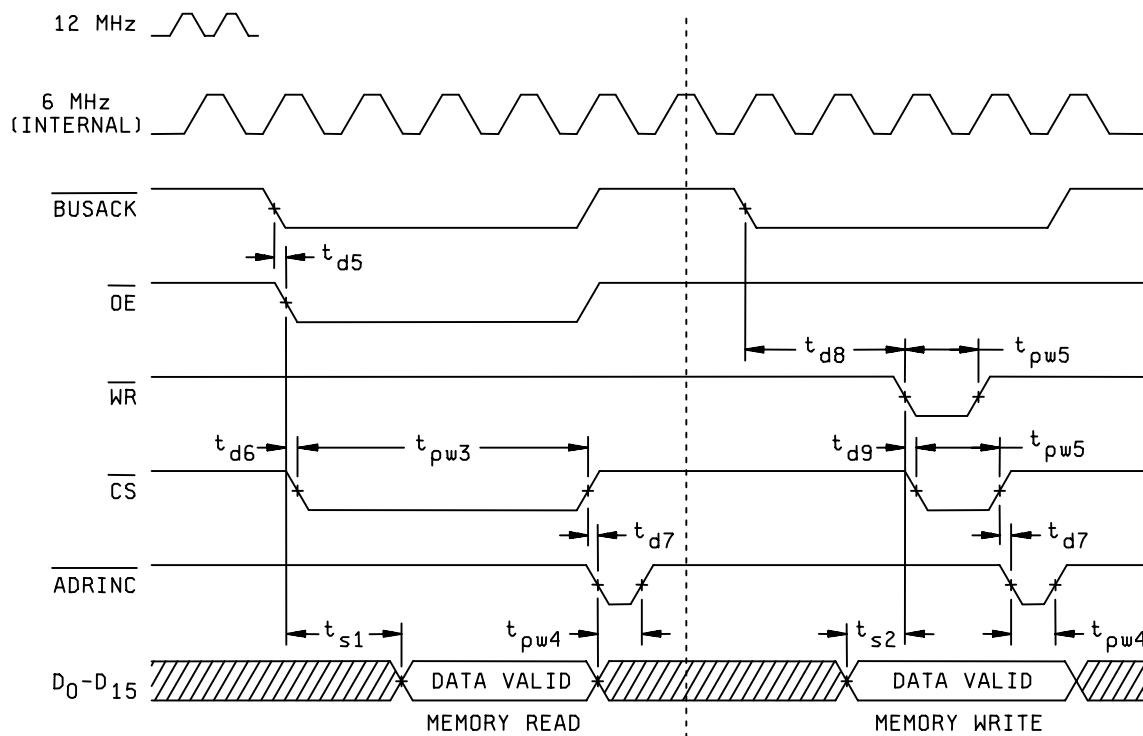


FIGURE 3. Timing diagram - BC read/write - Continued.

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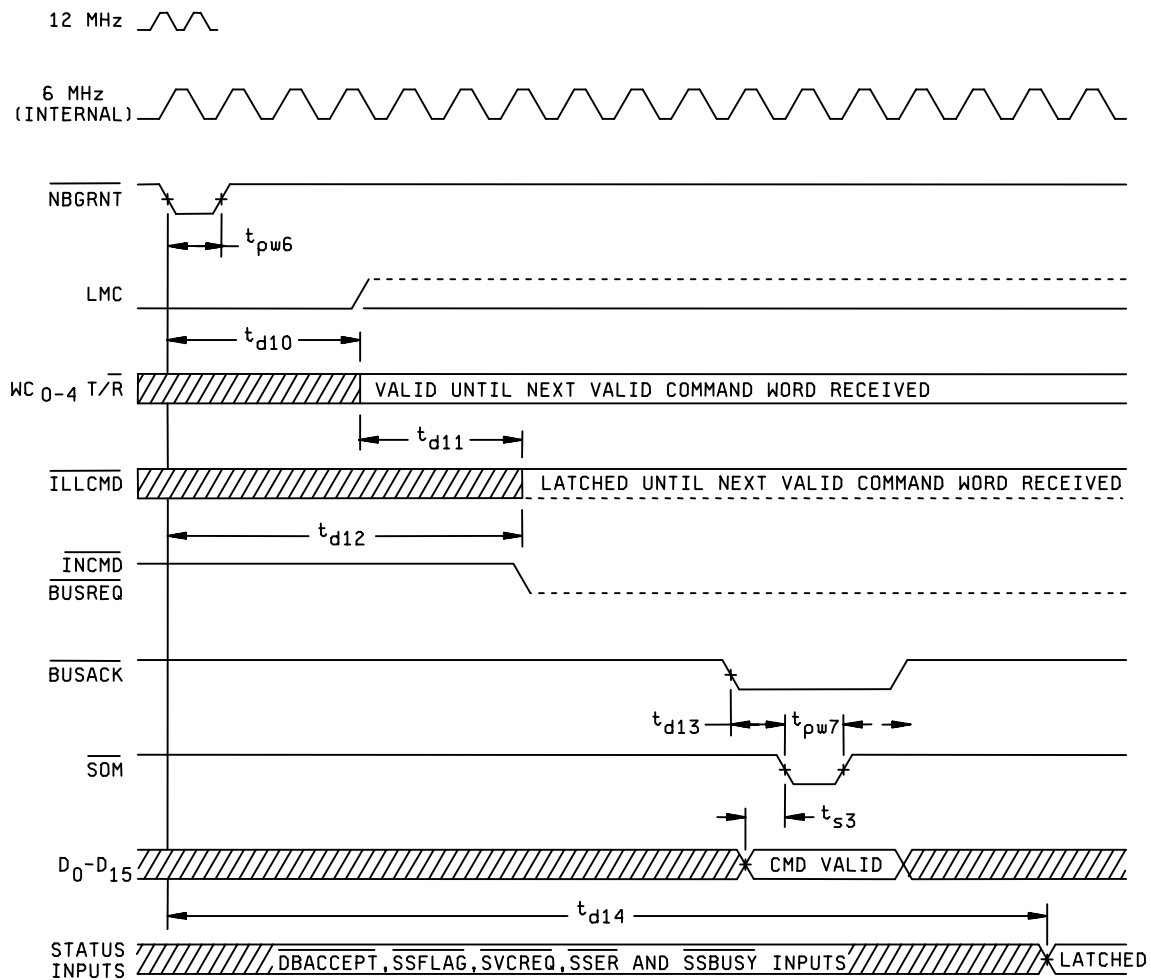


FIGURE 3. Timing diagram - RTU command word handling/status inputs - Continued.

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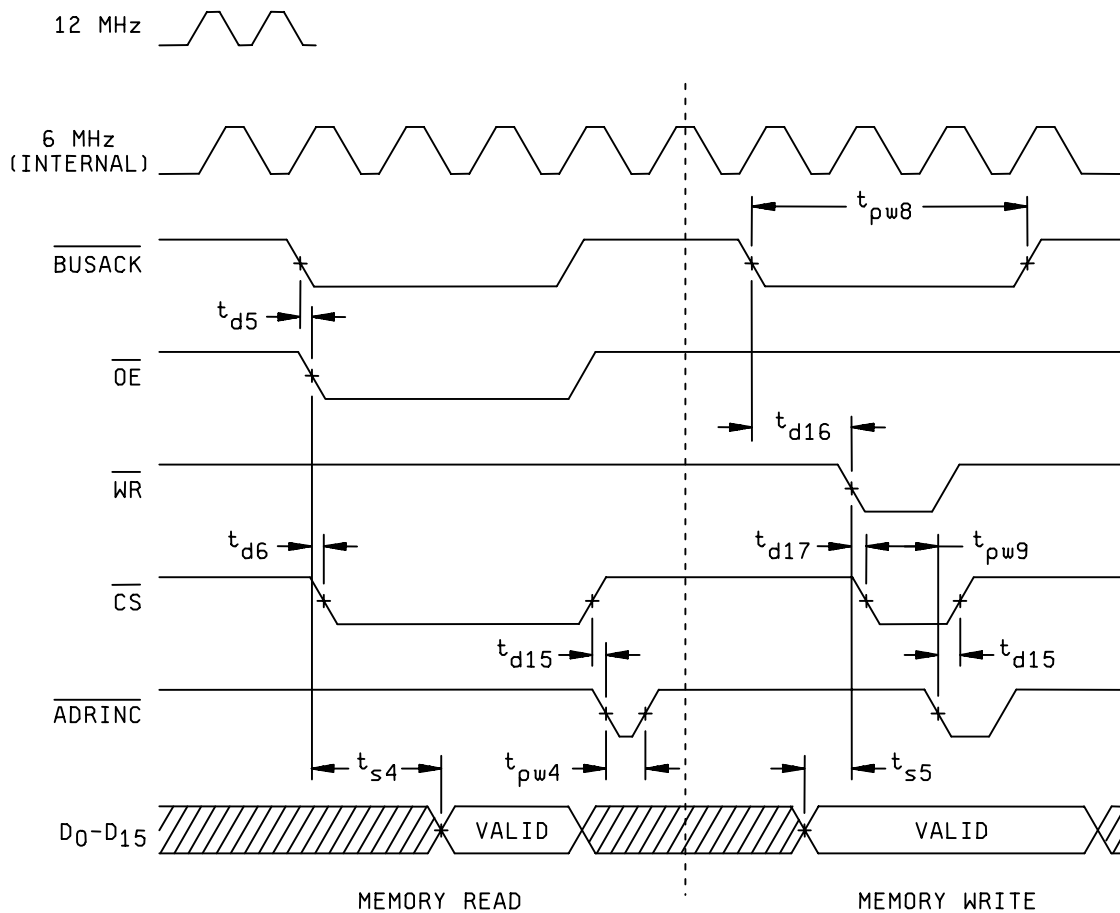


FIGURE 3. Timing diagram - RTU read/write - Continued.

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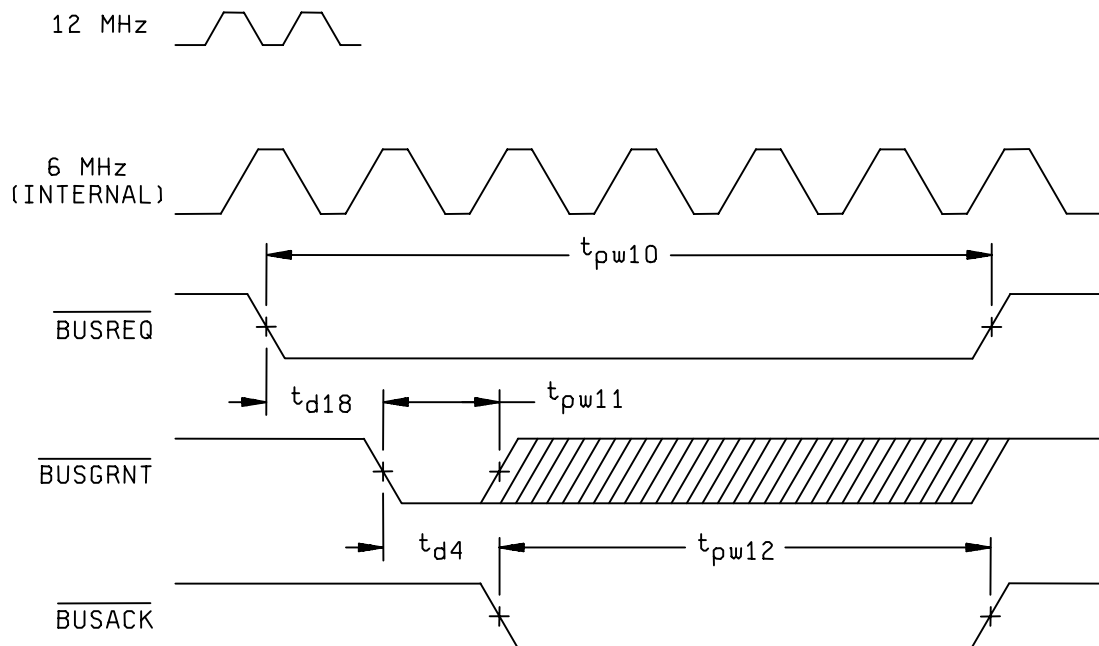


FIGURE 3. Timing diagram - BC handshake - Continued.

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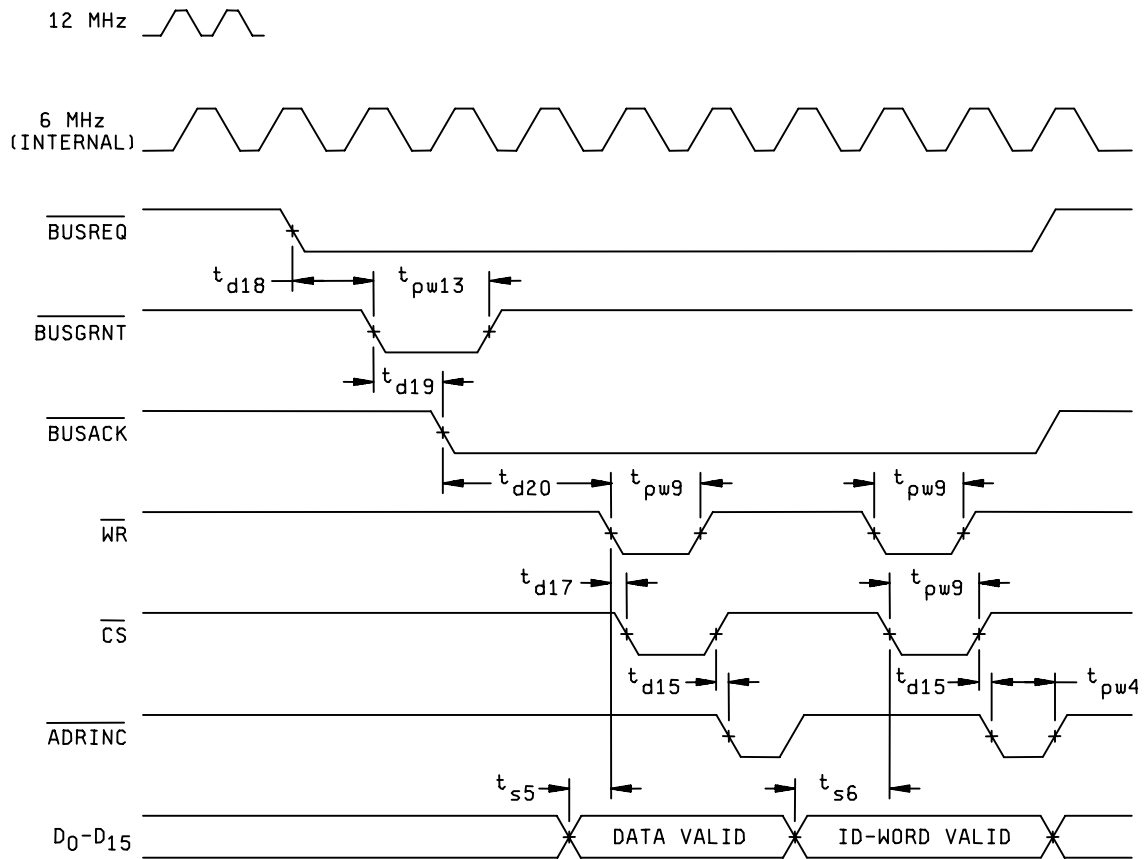


FIGURE 3. Timing diagram - MT transfer - Continued.

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TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1, 7, 9
Final electrical parameters	1*, 2, 3, 7*, 8, 9*, 10, 11
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3, 7, 8, 9, 10, 11
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	Not applicable

* PDA applies to subgroups 1, 7, and 9.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

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4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Pin functions. Microcircuits conforming to this drawing shall have pin functions as specified in table III herein.

TABLE III. Pin functions.

Pin name	I/O	Description
RT/ \overline{BC}	I	Remote Terminal/Bus controller. Logic "1" for RT mode, logic "0" for BC mode.
\overline{MT}	I	Bus monitor. Logic "0" for MT mode, Logic "1" for BC mode.
\overline{STATEN}	O	Status Enable. Indicates status word being transferred on internal bus.
$\overline{TIMEOUT}$	O	Indicates no response timeout has occurred during BC or RTU (RT to RT transfer).
\overline{HSFAIL}	O	Handshake failure. Indicates subsystem failed to grant a bus request (DMA handshake) within the required time period.
$\overline{DBACCEPT}$	I	Dynamic Bus Control Accept. Controls the DBACCEPT bit in RTU status word for response to valid mode command on 1553 bus.
\overline{SSFLAG}	I	Subsystem flag. Controls SSFLAG in RTU status word.
\overline{SVCREQ}	I	Service Request. Controls SVCREQ bit in RTU status word.
\overline{INCMD}	O	In Command. Indicates BC/RTU currently in message transfer sequence.
\overline{SSER}	I	Subsystem Error. Controls terminal flag bit in status word.

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TABLE III. Pin functions - Continued.

Pin name	I/O	Description
$\overline{\text{TESTOUT}}$	--	Factory test pin, no connection.
WC1	O	Word Count bit 1. Received from Command Word.
WC3	O	Word Count bit 3. Received from Command Word.
TXINH B	O	Transmitter Inhibit Channel B.
$\text{T}/\overline{\text{R}}$	O	Transmit/Receive. Indicates $\text{T}/\overline{\text{R}}$ bit of current Command Word in RTU mode.
$\overline{\text{CHA}}/\text{CHB}$	O	Channel A/Channel B. Indicates current selected channel.
$\overline{\text{CS}}$	O	Chip select. Used for external memory operations.
$\overline{\text{OE}}$	O	Output enable. Used for memory read operations.
$\overline{\text{BUSREQ}}$	O	Bus Request. Initiates handshaking prior to all subsystem transfers.
+ 5 V	I	+ 5 V dc input.
DB0 (LSB)	I/O	Data Bus Bit 0.
DB2	I/O	Data Bus Bit 2.
DB4	I/O	Data Bus Bit 4.
DB6	I/O	Data Bus Bit 6.
DB8	I/O	Data Bus Bit 8.
DB10	I/O	Data Bus Bit 10.
DB12	I/O	Data Bus Bit 12.
DB14	I/O	Data Bus Bit 14.
LWORD	--	For factory use only. Last word output in BC mode indicates last data word of current message transfer has been transferred on the data bus.
$\overline{\text{MSGERR}}$	O	Indicates error occurred during current message sequence in BC/RTU mode.
TXDATA A	O	Transmit data A. Data output to transceiver input.
$\overline{\text{RXDATA A}}$	I	Receive data A. Data input from transceiver.
RTADP	I	RT Address Parity Bit.
RTAD1	I	RT Address Bit 1.
RTAD3	I	RT Address Bit 3.
$\overline{\text{RESET}}$	I	Resets all unit parameters (200 ns minimum pulse).
TXDATA B	O	Transmit Data B. Data output to transmitter input.
$\overline{\text{RXDATA B}}$	I	Receive Data B. Data input from transceiver.
12 MHz	I	12 MHz TTL clock.
GND	--	Signal ground.
$\overline{\text{BCSTART}}$	I	Bus Controller Start. Initiates BC message transfer and begins $\overline{\text{MT}}$ operation (on rising edge).

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TABLE III. Pin functions - Continued.

Pin name	I/O	Description
$\overline{\text{NBGRNT}}$	O	New Bus Grant. Indicates start of message transfer sequence.
$\overline{\text{BITEN}}$	O	Built In Test Enable. Indicates RT transfer of BIT word on internal 16 bit bus.
$\overline{\text{WR}}$	O	Write Enable. Enables memory write operation from unit.
$\overline{\text{BUSGRNT}}$	I	Bus Grant. Response to $\overline{\text{BUSREQ}}$ output. (DMA-type handshake).
$\overline{\text{LOOPERR}}$	O	Loop Error. Logic "0" indicates failure during loop back of last transmitted data in BC/RTU mode.
$\overline{\text{SSBUSY}}$	I	Subsystem Busy. Controls the (Subsystem) Busy Bit in status word
$\overline{\text{ILLCMD}}$	I	Illegal Command. Used to block RT response to illegal command.
$\overline{\text{ADRINC}}$	O	Address Increment. Low level pulse which returns high after the rising edge of CS (memory read/write). Used to increment external address counter.
CHASSIS	--	Chassis ground.
WC0	O	Word Count Bit 0. Received from Command Word.
WC2	O	Word Count Bit 2. Received from Command Word.
WC4	O	Word Count Bit 4. Received from Command Word.
TXINH A	O	Transmitter Inhibit Channel A.
LMC	O	Latched Mode Command. Logic "1" indicates current command word is a mode code; WC0 through WC4 specifies mode.
$\overline{\text{TESTIN}}$	--	Factory test input-enable fail safe counter for selected channel.
$\overline{\text{EOM}}$	O	End of Message. Logic "0" (pulse) occurs when BC/RTU message is completed.
$\overline{\text{BUFENA}}$	I	Buffer Enable. May be driven low during STATEN or BITEN low. Allows subsystem to read status or BIT words. Enables internal 16 bit bus onto subsystem bus.
$\overline{\text{BUSACK}}$	O	Bus Acknowledge. Low during DMA handshake, in response to $\overline{\text{BUSGRNT}}$.
DB1	I/O	Data Bus Bit 1.
DB3	I/O	Data Bus Bit 3.
DB5	I/O	Data Bus Bit 5.
DB7	I/O	Data Bus Bit 7.
DB9	I/O	Data Bus Bit 9.
DB11	I/O	Data Bus Bit 11.
DB13	I/O	Data Bus Bit 13.
DB15 (MSB)	I/O	Data Bus Bit 15.
$\overline{\text{STATERR}}$	O	Status error. Indicates one or more bits set or address mismatch in received status word.
$\overline{\text{TXDATA A}}$	O	Transmit Data A. Data output to transceiver input.
$\overline{\text{RXDATA A}}$	I	Receive Data A. Data input from transceiver.

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TABLE III. Pin functions - Continued.

Pin name	I/O	Description
$\overline{\text{NO DT}}$	O	No Data. Logic "0" indicates idle 1553, Logic "1" indicates selected bus channel active.
RTAD0	I	RT Address Bit 0.
RTAD2	I	RT Address Bit 2.
RTAD4	I	RT Address Bit 4.
$\overline{\text{BCSTRCV}}$	O	Broadcast Receive. Indicates current command is broadcast.
TXDATA B	O	Transmit Data B. Data output to transmitter input.
$\overline{\text{RXDATA B}}$	I	Receive Data B. Data input from transceiver.
$\overline{\text{SOM}}$	O	Start of message. Indicates Command Word available to subsystem on parallel data bus. Active during the Command Word DMA handshake period.

6.4 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.5 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.6 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.7 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-02-25

Approved sources of supply for SMD 5962-88585 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8858501XA 5962-8858501XA 5962-8858501XC 5962-8858501XC	<u>3/</u> 88379 <u>3/</u> 88379	BUS-65600-883B CT2565-001-2 BUS-65600-883B CT2565-001-1
5962-8858501YA 5962-8858501YA 5962-8858501YC 5962-8858501YC	<u>3/</u> 88379 <u>3/</u> 88379	BUS-65601-883B CT2565-201-2 BUS-65601-883B CT2565-201-1
5962-8858502XA 5962-8858502XC 5962-8858502YA 5962-8858502YC	88379 88379 88379 88379	CT2565-002-2 CT2565-002-1 CT2565-202-2 CT2565-202-1

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ No longer available.

Vendor CAGE
number

88379

Vendor name
and address

Aeroflex Circuit Technology Corporation
35 South Service Road
Plainview, NY 11803

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.